Chapter – 7
Circuit Design

From symbols to substance

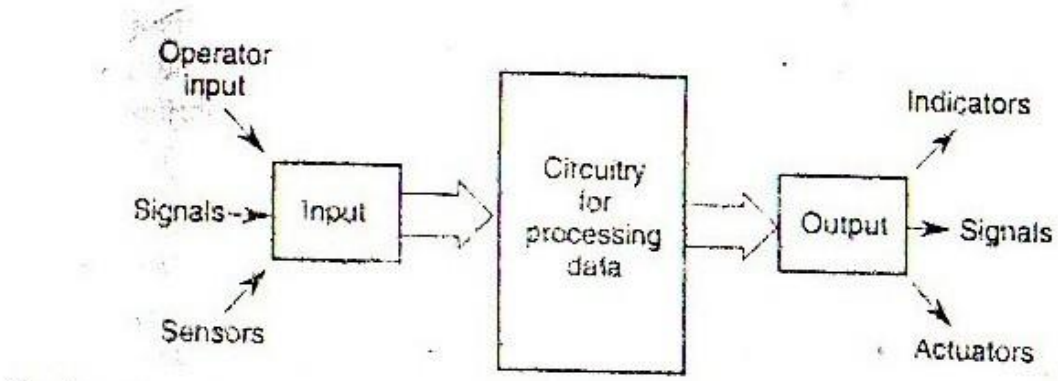


Fig. 7.1 General configuration for the circuits within a system.

7.1 Converting requirement into design

- Establishing requirement is the most difficult part of the circuit design.
- Experience is the best guide for setting requirements
- General to specific approach of establishing requirements:
  - Start by defining the desired function in broad term
  - Redefine the function with operational concerns
  - Settle on exact regulations and specification
- Setting specifications is one of the most difficult parts of engineering where good judgment and experience are necessary.
- Requirements often change late in the effort and spoil the design
- Some principles bound the design problem
  - E.g. use of electromagnetic spectrum
- Time and effort in design increases as the complexity of the function of system increases
- Choice of certain technology and devices are the result of good analysis and may depend on different factors
  - E.g. choice of a microprocessor for a system
  - Choice of A/D and D/A converters
- Technology drives the requirements. Audio frequency (~KHz) → Discrete components, wirewrap or PCB. Radio frequency (~MHz) → PCB (transmission line effect). Microwave frequency (~GHz) → RF design (Geometric structures).
- **Throughput:** The average rate of successful message delivers over a communication channel.
- Knowing region of operation, we can pick option available for circuit design. Right choice → Part count (↓), board apace (↓), Power (↓), Cost (↓), time to market (↓), reliability (↑).

Table 7.1 Some requirements that drive design

System concern	Requirement	Parameters
Function	Response times	s, min, hr
	Data rates	Mbytes/s, kbits/s
	I/O drive	A, V
	Reliability—MTBF	hr
Regulations	FCC	
	UL	
	Military specifications	
Environment	Volume	in^3, m^3
	Weight (mass)	lb, kg
	Vibration	g, m/s^2
	Shock	g, m/s^2
Operation	Bandwidth	Hz
	Resolution	%, mV/LSB
	Speed	ns, μs, ms
	Accuracy	%
	Power consumption	mW
	Noise	$nV/\sqrt{Hz}$, SNR

Note: FCC = Federal Communications Commission; LSB = least significant bit; MTBF = mean time between failures; SNR = signal-to-noise ratio; UL = Underwriters Laboratories.

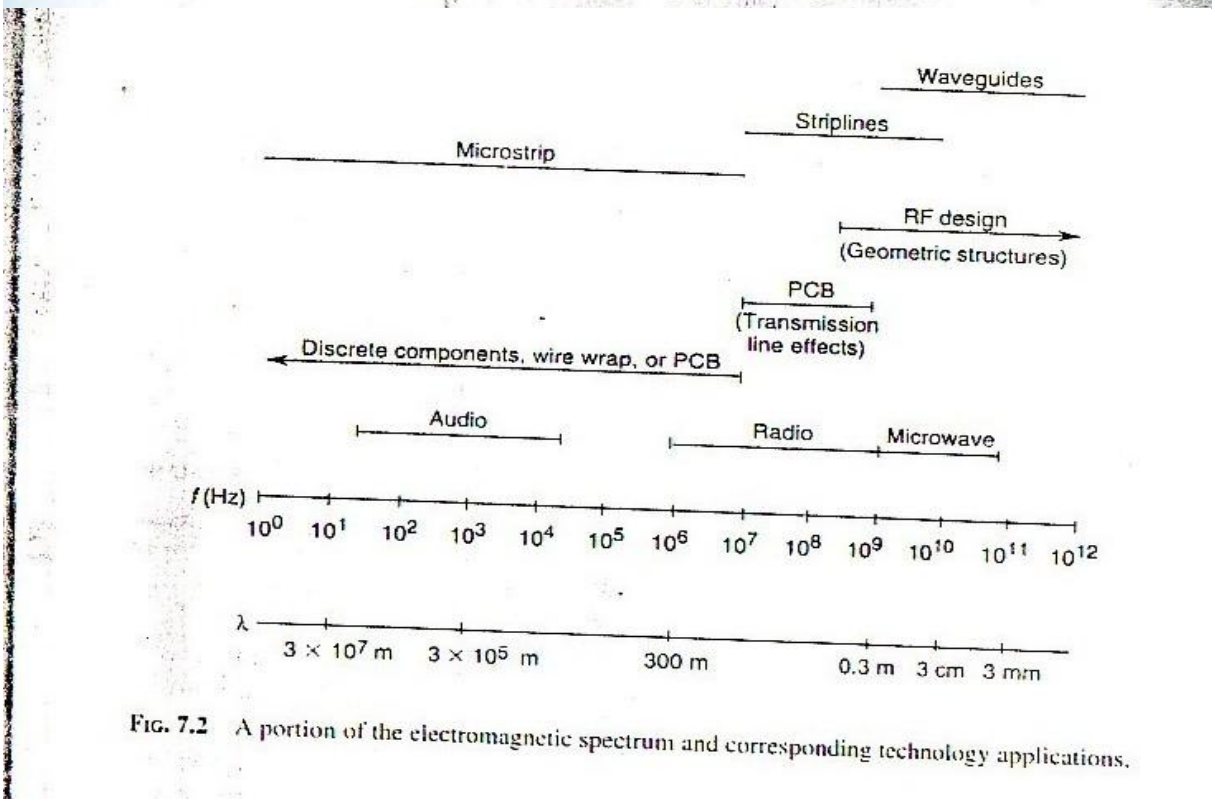


FIG. 7.2 A portion of the electromagnetic spectrum and corresponding technology applications.

ASIC (Application Specific Integrated Circuits)

- It is an IC customized for particular use. For an example chips designed solely to run cell phones.
- Modern ASIC includes → 32 bit processor, ROM, RAM etc. Such ASIC are called System on Chip (SOC).
- Solve signal/data processing problems optimally in terms of high throughput and low power.
- Low cost but takes longer time to market.

Standard Cells

- Group of transistors are interconnected structures that provides Boolean logic function or storage function.
- Simplest cells are direct representatives of adder, mux, flip-flops etc.

Gate Array

- Analogous to Cu layer of PCB.
- Transistors, standard NAND, NOR gates placed at predefined position and manufactured in wafer.
- Late manufacture process → joined to logic as desired shorter time to market.

Programmable Logic Array (PLA)

- Implement combinational logic
- Set of programmable AND gates which link to set of programmable OR gates

Programmable Logic Device (PLD)

- To build reconfigurable logic circuits
- E.g. ROM → store i/p logic as address; o/p logic → store in ROM

Programmable Array Logic (PAL)

- Fixed OR with programmable AND
- O/P logic → registered or combinational

Electrically PLD (EPLD) or Complex PLD (CPLD)

- Non volatile configuration memory
- Can implement complex logics

Field Programmable Gate Array (FPGA)

- Field → firmware can be modified in field without dissembling device or returning into manufacturer
- IC designed to configure by customer or designer after manufacture
- Programmable logic components called logic blocks wired together to form complex logic plus it has analog features → programmable slew rates
- Uses HDL (hardware descriptive language) to implement logic functions.
- Low non-recurrent engineering cost but high unit cost in comparison to ASIC
- Logic blocks plus embedded microprocessor to form complex system on programmable chips.

- Software processor → implemented within FPGA logic; highly configurable and flexible than hardwire processor
- Applications: DSP, aerospace, ASIC, prototyping, medical imaging etc.
- Short time to market
- Flexibility in both hardware and software

Technology	Performance/Cost	Time to market
ASIC	Very high	Very long
Custom processor or DSP	Medium	Long
FPGA	Low-medium	Short
Generic logic	Low-medium	Short

Microcontrollers

- CPU, I/O devices, program memory, data memory all in single chip

Microprocessors

- Requires other parts to make workable computer.

Selection of microprocessor / Microcomputer

1. Experience
2. Software dependent tools for particular processor
3. Performance: Architecture dependent
4. No. of peripheral function
5. Memory
6. Tools support to determine the appropriate processor
7. Low power consumption

Performance is determined by

- Throughput
- Resolution
- Address space and available memory
- Language choice, code size, speed
- Predominant types of calculation: integer and floating point

No. of peripheral function

- Math coprocessor
- Graphics accelerator
- Interrupt handler
- Data transfer and communication: DMA, small computer system interface(SCSI), Serial I/O Ports
- Timer
- ADC and DAC
- Power drivers
- Watchdog timing (System reset in case of system unresponsiveness)

Memory

- Require minimum size of memory
- Always plan for and specify margin in the requirements for future updates and modifications.
- Size of RAM/ROM Depends on
  - Data array
  - Stack
  - Temporary and permanent variable
  - Compiler overhead
  - I/O buffer

Tools support to determine the appropriate processor

- Hardware emulator: Helps to debug both circuits and code
- Software tools: supports development on the selected processor
- Vendor: good support, good reputation, markedly affected development tools

Power consumption within a processor

- Cooling concerns
- Battery sizing

Complexity vs. Right Technology

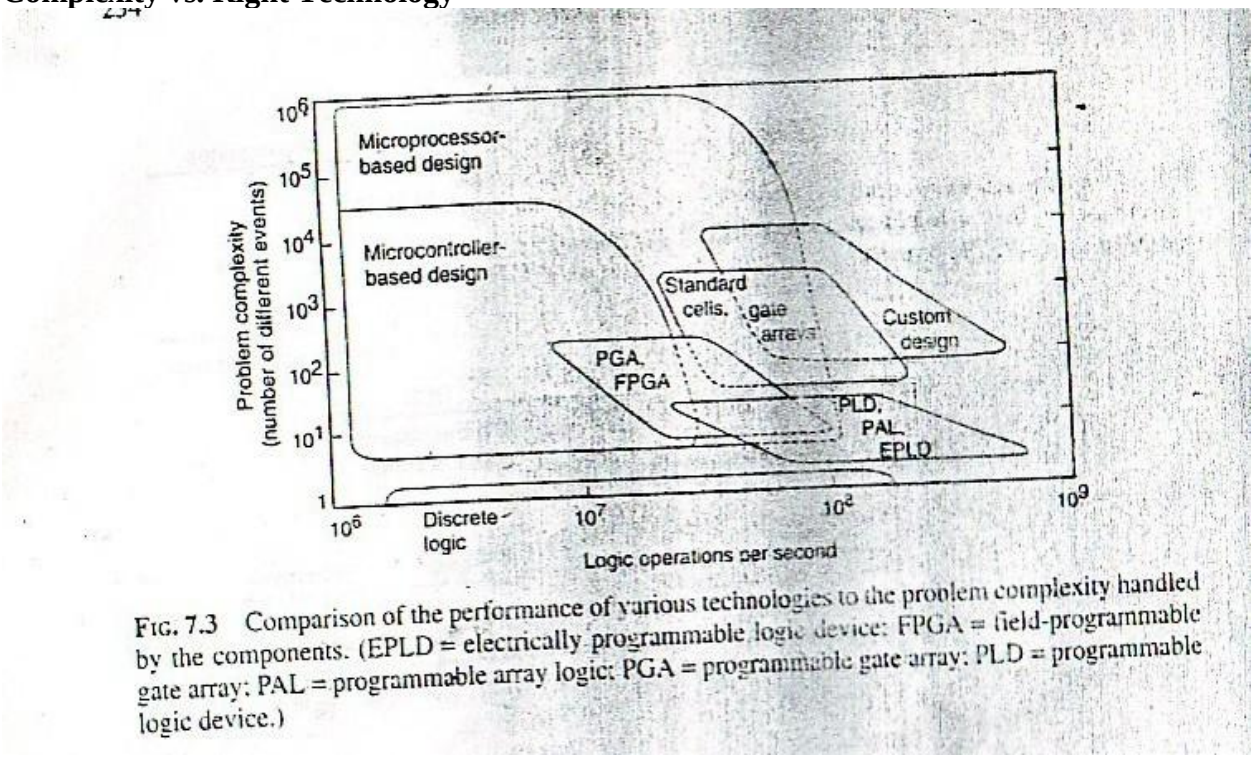


FIG. 7.3 Comparison of the performance of various technologies to the problem complexity handled by the components. (EPLD = electrically programmable logic device; FPGA = field-programmable gate array; PAL = programmable array logic; PGA = programmable gate array; PLD = programmable logic device.)

Design time vs. Complexity

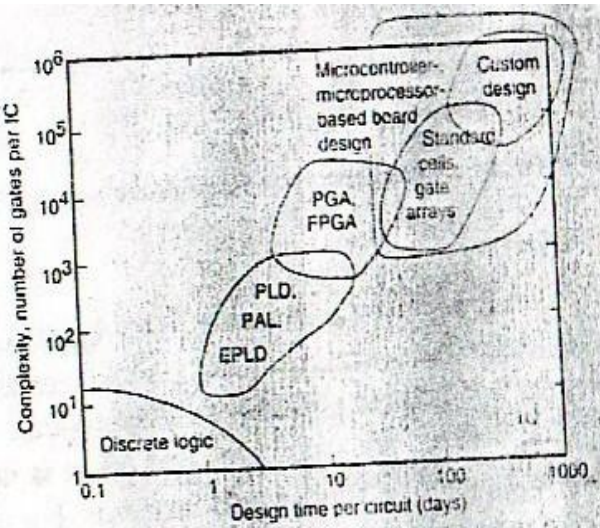


FIG. 7.4 Comparison of the design time required using various technologies versus the complexity of the components.

7.2 Reliability, fault tolerance

Reliability

- How long the product will last?
- Two factors role in the reliability:-
  - Complexity:- Fewer part better
  - Design margin:- We must allow for stressing of components
- Two methods to measure reliability:-
  - Model prediction:- help update estimates of reliability but are limited and cannot predict every outcome
  - Prototype test:- find out many weaknesses and problems but are time consuming
- Combination of both is mostly used
- Standard methods for modeling use formulas based on practical experience of failure rates and physical knowledge to relate environmental factors to the reliability of electronic components.
- The failure rate for a component is a generally a base rate modified by various factors
  $\lambda = \lambda_b \pi_e \pi_q \pi_a$ ……..(1)
  Where, λ = failure rate, λ_b = base failure rate
  π_e = environmental factor, π_q = quality factor
  π_a = acceleration factor
- Reliability of a component is a function of failure rate:
  $R(t) = e^{-\lambda t}$ ……..(2)
  Where R(t) = Reliability, λ = failure rate, t = time

- Reliability of a System is a product of all component reliabilities:

  $R_{System} = \prod_{i=1}^{n} Ri$ ……..(3)

  Where R_{system} = reliability of the system, R_i = reliability of component
- Most failure rates relate acceleration factors (π_e, π_q, and π_a) to temperature, but not its applications.
- We may consider the application and some of the stresses and susceptibility factors might affect reliability
  - Corrosion, Thermal cracks, Electro migration, Secondary diffusion, Ionizing radiation, Vibration, High voltage breakdown, Ageing
- These can drastically alter reliability and still not predicted by standard models.

Fault tolerance

- Goes beyond the design and analysis for reliable operation and reduces the possibility of dysfunction or damage from abnormal stresses and failures.
- Allows a measure of continued operation in the event of problem
- Three distinct area
  - Careful design
  - Testable function
  - Redundant Architecture

Careful Design

- Careful design can avoid many failures from abnormal stresses. Some design techniques that can reduce the probability of failure:
  - Reduce overstress from heat with cooling and low dissipation design.
  - Use optoisolation or transformer coupling to stop overvoltage and leakage current
  - Implement ESD protection
  - Mount for shock and vibration
  - Tie down wires and cables
  - Prevent incorrect hookup; Use keyed connector

Testable Architecture

- The process of testing and diagnosing failures within a system.
- Two possible configurations of testable architecture:
  - **Simple Configuration:** Provides Probe points / test points for a technician or instrument to stimulate circuits and record responses. Only the trained personnel must disassemble the system and remove the circuit for testing.
  - **Complex Configuration:** Dedicated internal circuitry called built in test (BIT) that tests the system and diagnoses problems without disassembly of the equipment so adds complexity and reduces reliability. The trade off for BIT is quicker diagnoses and repair versus higher reliability.
- An appropriate calibration standard is always necessary when you measure a result.

Redundant Architecture

The most complex and fault tolerant architecture are redundant architectures. They use multiple copies of circuitry and software to self check between functions. It is justified only when downtime for repair and maintenance cannot be tolerated.

- **Doubly redundant architecture**: merely indicates a failure in one of the subsystems; this allows for quick repair.
- **Triply redundant architecture**: uses voting between the outputs of three identical modules to select the correct value. It can have failure and still operate correctly.
- **Dissimilar redundancy**: compares the output from modules with different software and hardware to select the correct value. It can survive failure and even indicate errors in design if one system is coded correctly and the others are not.

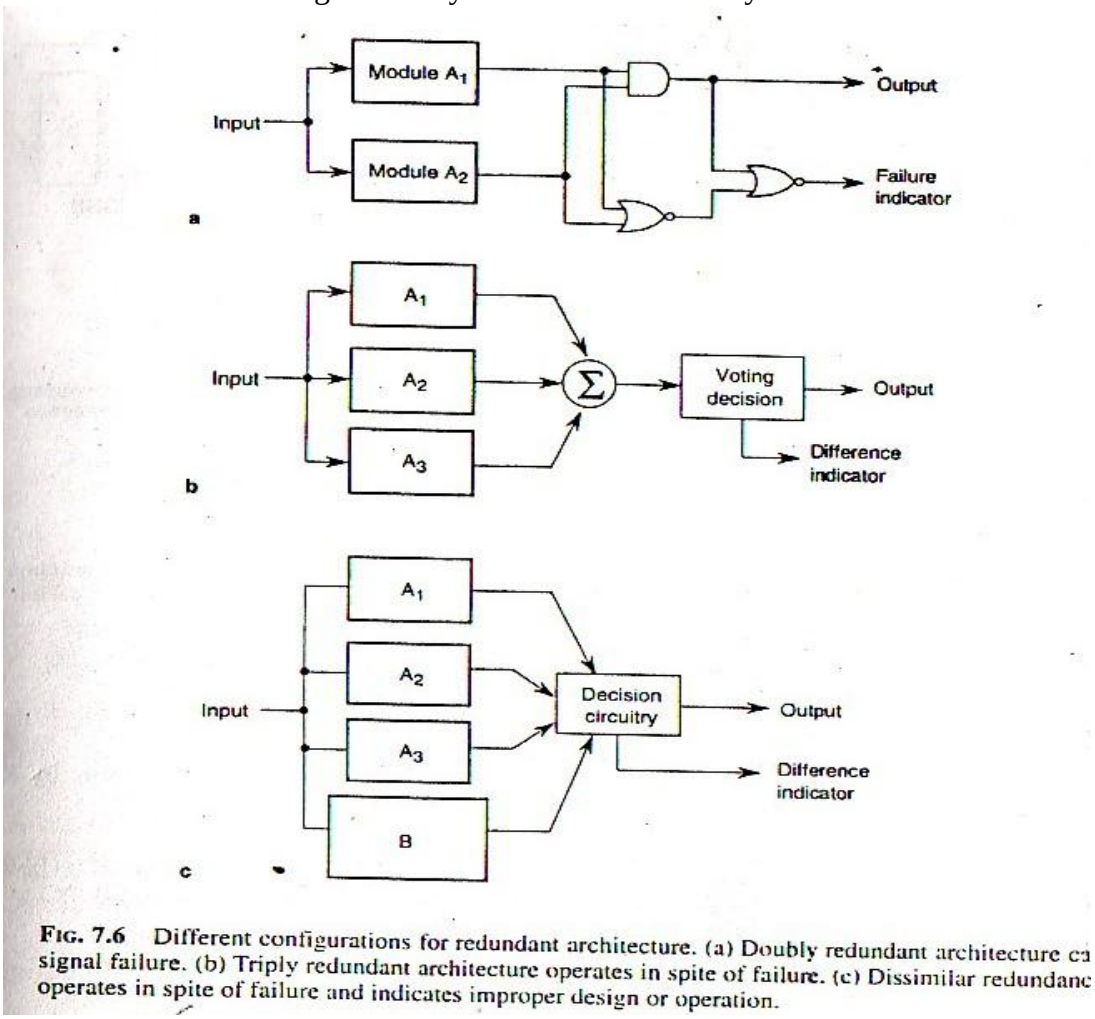


FIG. 7.6 Different configurations for redundant architecture. (a) Doubly redundant architecture ca signal failure. (b) Triply redundant architecture operates in spite of failure. (c) Dissimilar redundanc operates in spite of failure and indicates improper design or operation.

7.3 High speed design

- We should consider transmission line effect when clock of frequency exceeds 1 MHz in a circuit or system because the harmonics generated by the edges of the clock and signal pulses can easily be 20 or 30 times the fundamental.
- Two conservative criteria may be used to estimate when transmission line effect begins

  - **Circuit dimension Vs signal wavelength**: If circuit dimension exceed 5% of the minimum wavelength, then signal path approaches a transmission line i.e. $\boldsymbol{l > \lambda/20}$ where, l = length of signal path, λ = maximum wavelength of the signal.
  - **Rise time Vs propagation delay**: If the rise time of a signal is less than 4 times the propagation delay of the signal path, then the signal path approximates a transmission line with a characteristic impedance i.e. $\boldsymbol{t_r < 4t_p}$ where, t_r = rise time of signal, t_p = propagation delay of the signal path.
- Transmission line problems:- BW, decoupling, ground debounce, crosstalk, impedance mismatch and timing skew or delay

7.3.1 Bandwidth, Decoupling, ground bounce, cross talk, Impedance matching and timing

Bandwidth

- Limiting the bandwidth of the signals within a system is the most effective way to reduce noise, EMI and problems with transmission lines.
- May limit the bandwidth either by increasing the rise or fall times of the signal edges or by reducing the clock frequency.
- Selecting the appropriate logic family will set the edge rates and the consequent limit on transmission line concerns.
- One criterion for selecting logic according to transmission line effects is a ratio less than 4 between the rise time, t_r and the propagation delay, t_p i.e. (tr/tp <4).
- Slower edge rates allow longer interconnections between circuits.

Decoupling

- Switching of digital logic causes transients of current on the voltage supply through inductive impedance of the circuit
- Decoupling capacitor minimizes inductive loop area thus reducing impedance of power supply circuit. Shortest possible path for decoupling capacitor is best.

General recommendation for Decoupling:

- Use decoupling capacitor near each chip for two sided board
- Use a large filter capacitor at the power entry point
- Use a ferrite bead at the power entry point to the circuit board

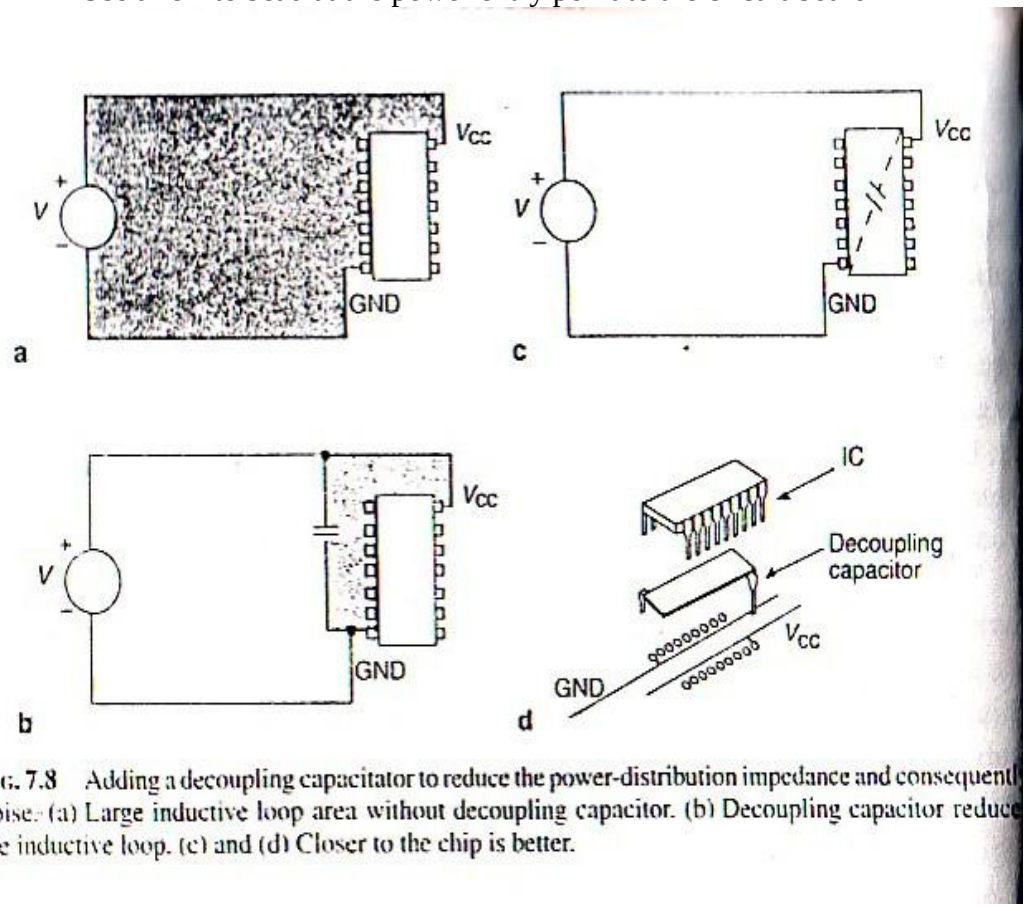


FIG. 7.8 Adding a decoupling capacitator to reduce the power-distribution impedance and consequentl noise: (a) Large inductive loop area without decoupling capacitor. (b) Decoupling capacitor reduce the inductive loop. (c) and (d) Closer to the chip is better.

Ground Bounce

- Ground bounce is a voltage surge that couples through the ground leads of a chip into non switching output and injects glitches onto signal lines.
- Asynchronous signals are more prone to ground bounce.
- Can reduce ground bounce by:
  - Reducing loop inductance
  - Reducing input gate capacitance
  - Choosing logic families that either control the signal transition or have slower fall times.

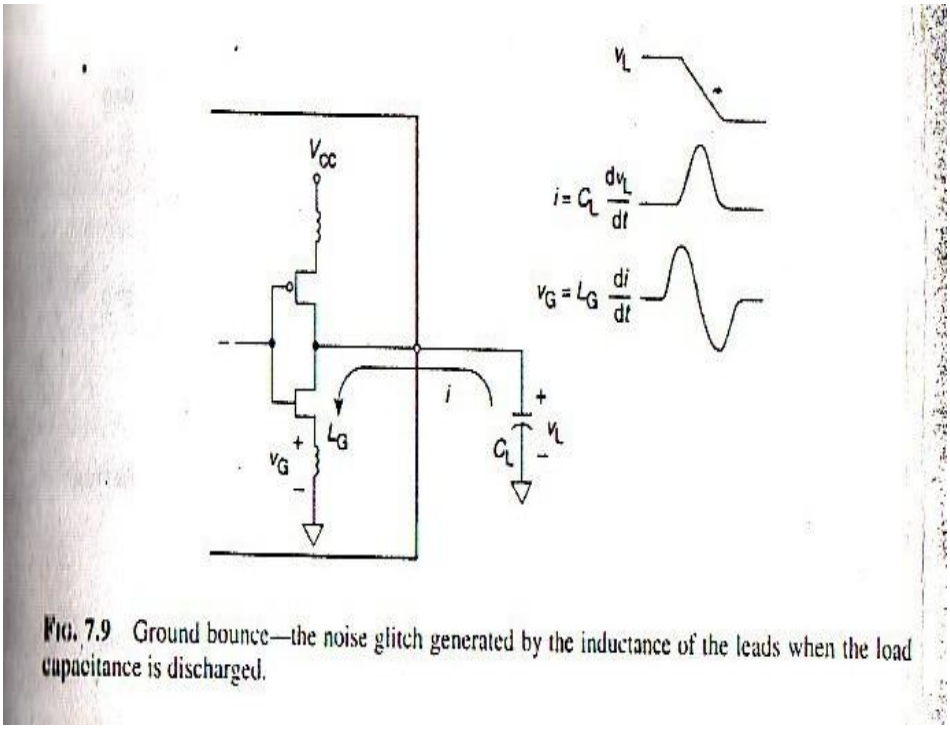


FIG. 7.9 Ground bounce—the noise glitch generated by the inductance of the leads when the load capacitance is discharged.

Crosstalk

- Coupling electromagnetic energy from an active signal to a passive line
- Coupling mechanism:- capacitive or inductive
- Depends on line spacing, length and characteristic impedance, signal rise times
- To reduce crosstalk:
  - Decrease coupling length and characteristic impedance
  - Increase rise time of signal
  - Better layout and design of circuits

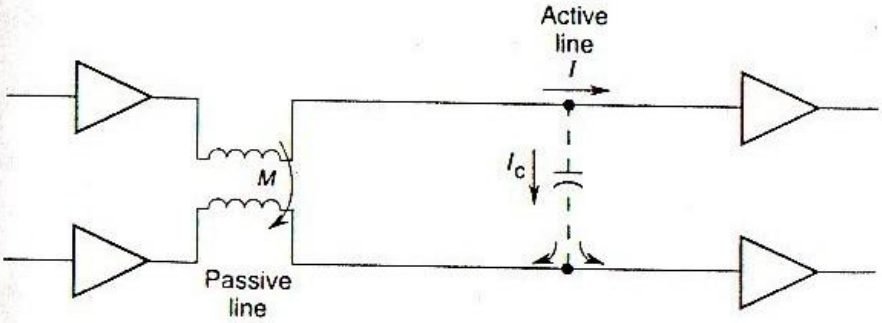


FIG. 7.10 Crosstalk—the inductive and capacitive coupling of signal from an active line to a passive line. (M = mutual inductance; I_c = capacitive current.)

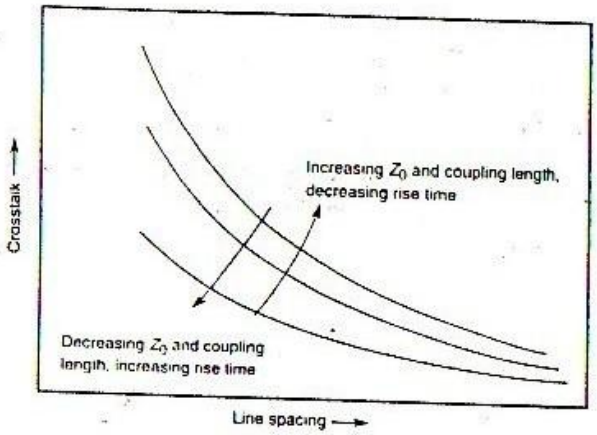


FIG. 7.11 Relationship of crosstalk to line spacing, coupling length, characteristic impedance (Z_0), and signal rise times.

Avoiding Crosstalk

- Don't run parallel traces for long distances – particularly asynchronous signal
- Increase separation between conductors
- Shield clock lines with ground strips
- Reduce magnetic coupling by reducing the loop area of circuits
- Sandwich signal lines between return planes
- Isolate the clock, chip-select, chip-enable, read and write lines

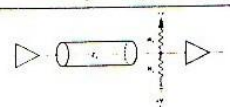
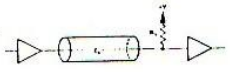
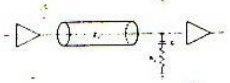
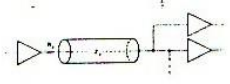
Impedance matching

- The reflection coefficient for a signal passing from medium 1 to medium 2 is given by:
  $\tau = (\eta_2 - \eta_1) / (\eta_2 + \eta_1)$
  Where η_i is the intrinsic impedance of medium i and is given by:
  $\eta_i = \sqrt{\mu i / \varepsilon i}$
- Reflection coefficient will be zero when $\eta_1 = \eta_2$
- Impedance matching makes the source and termination impedance equal to the characteristic impedance of the transmission line so that it will eliminate the reflections of signals that cause ringing (oscillations), undershoot, and overshoot in the signal pulses.
- Impedance discontinuities occur in two configurations endpoint and stub.

End point discontinuity: - the ends of the transmission line don't match its characteristic impedance of the transmission line.

- Add series resistances at the end until the total impedance equals the line impedance.
- Terminate the other end of the signal line from driver.

Table 7.3 Several methods to terminate signal lines by impedance matching, $Z_0 = Z_L$

Terminating configuration	Load impedance, Z_L	Advantages	Disadvantages
	$R_1 \| R_2$, assuming $Z_{receiver} \approx \infty$ otherwise $R_1 \| R_2 \| Z_{receiver}$	Active termination voltage to help a weak driver by speeding transitions. Use with TTL, FAST, and ECL logic.	Constant DC power dissipated through R_1 and R_2. More components required.
	R_1 or $R_1 \| Z_{receiver}$	Reduces DC power dissipation.	Additional load will slow weak drivers.
	R_2 or $R_2 \| Z_{receiver}$	Reduces DC power dissipation	Additional load will slow weak drivers.
	R_2 or $R_2 \| Z_{receiver}$ because $Z_c = 0$	Eliminates DC power dissipation. Use with FACT logic.	More components required.
	Source impedance $Z_S = R_S + Z_{driver}$	Allows branching at load. Eliminates DC power dissipation. Use with FACT and ECL logic.	
	R_1 or $R_1 \| Z_{receiver}$	Use with RS-422 and RS-485.	Constant DC power dissipated through R_L.
	R_1 or $R_1 \| Z_{receiver}$ because $Z_c = 0$	Eliminates DC power dissipation.	Long strings of consecutive 1's or 0's will charge C and cause time jitter in signal transition as C discharges.
	$2R_1$ or $2R_1 \| Z_{receiver}$	Reduces common-mode noise.	Constant DC power dissipated through resistors.

Note: Z_0 = characteristic impedance; Z_S = source impedance; Z_c = capacitive impedance.

Stub discontinuities cause impedance mismatch and signal reflection by connecting multiple circuits to a single line.

- Each Connection of a stub divides the impedance and splits the power of the signal
- Make them very short, even zero to reduce the effect of stub discontinuities
- Good layout and design

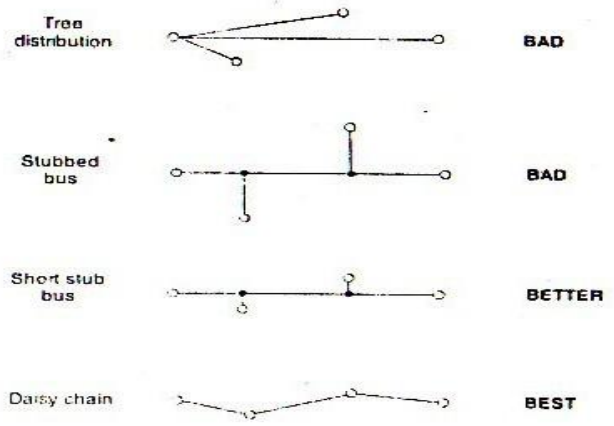


FIG. 7.12 Network geometries. Stubs cause signal reflections on transmission lines that result ringing, overshoot, and undershoot. Reduce the length of stubs and terminate the ends of the transmiss line to eliminate reflections.

Timing

- Clock frequency increases, propagation delays, timing skew, and phase jitter (change in phase) render logic design useless.
- Clock signal is skewed or arrived at different propagation delays of the clock signal to different destinations (propagation delay → different clock signal to arrive at different time).
- Differences in propagation delay of rising and falling edges change the duty cycle of the signal or shrink/expand it.
- Adequate setup and hold time is required to latch data reliably.

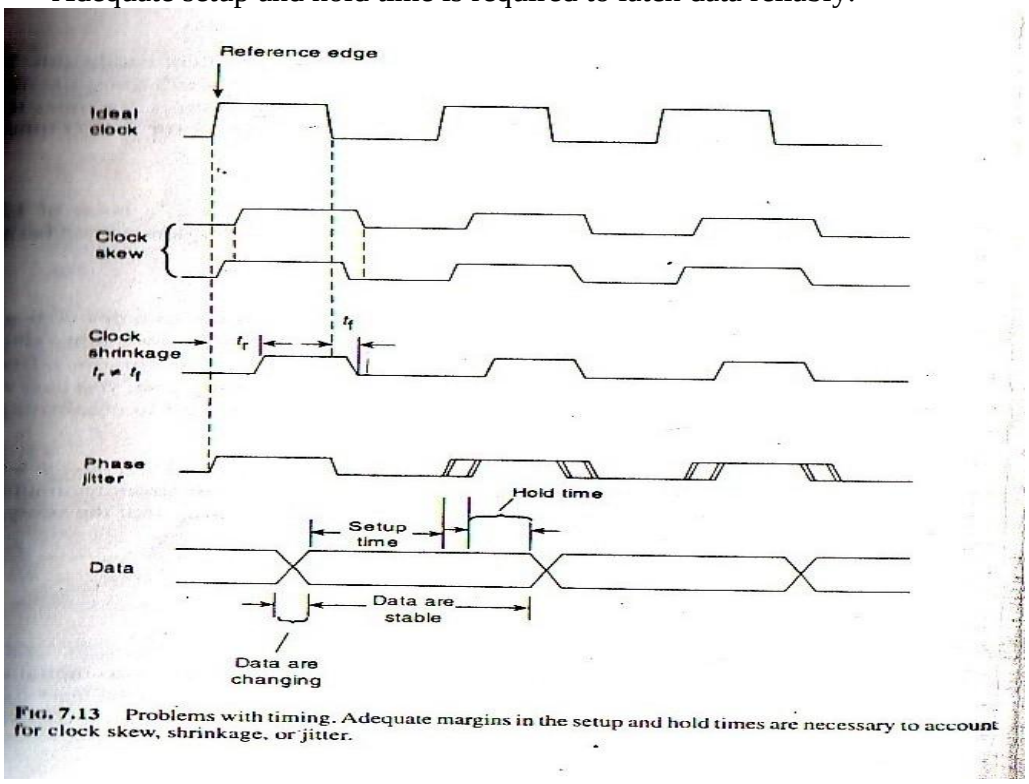


FIG. 7.13 Problems with timing. Adequate margins in the setup and hold times are necessary to account for clock skew, shrinkage, or jitter.

Standard data bus and networks

- Data bus or network is required to communicate with other circuit boards or devices
  - Bus Architecture
  - Serial communication
  - Instrumentation and I/O buses
  - Back-plane buses
- Backbone of design
- Represents a significant portion of system architecture

Bus architecture concerns:

- Drive configuration
  - Single ended:-
    - uses one trace or signal line for transmitted signal and shares circuit ground for return signal,
    - used for shorter paths:- e.g. on PCBs and RS 232 serial lines
  - Differential:-
    - transmits two signals with reversed polarity on two separate lines,
    - greater tolerance for noise than single ended as they reject common mode noise,
    - better for long cable
- Terminations
  - Multiple outputs of transistors connected in parallel present a considerable capacitive load and slows the transition time of signal
  - Use Scotty diodes which has low series capacitance
- Handshakes
  - Synchronous buses shares a common clock signal and asynchronous buses use handshake signals.

7.4 Low power design

- Design practices that reduce power consumption by at least one order of magnitude; in practice 50% reduction is often acceptable.
- Mobile, TV remote controls ,digital multimeter, video cameras, laptops used low power for Portability, Isolation, Battery power and low heat dissipation
- Power is function of frequency, load capacitance, and voltage reduction of any of these reduce power consumption.

Ppower (P) = f * C * V^2 *where f is the switching frequency, C is the load capacitance, and V is the DC supply voltage*

- Reduce power by reducing
  - Supply voltage
  - Clock frequency
  - Load capacitance
- These seven guidelines in design will minimize power
  1. Lower clock frequency
  2. Lower supply voltage to digital circuit
  3. Shut down unused circuits
  4. Sleep mode in case of not used

5. Terminate all unused inputs
6. Avoid slow signal transition
7. Make normal state use the lowest current, for instance LEDs should be off

Noise and Error Budgets

- Error 1 → Production variation, tolerance of resistors, capacitors
- Error 2 → Environmental factors e.g. temperature
- Error 3 → Noise within each devise

Types of Noise and error budgets:

1) Johnson or Thermal noise
   - Has a flat power spectrum and is "white" Gaussian noise

   $V_{noise}\,(rms) = \sqrt{4KTRW}$

   Where, K = the Boltzmann constant = $1.38X10^{-23}$ J/K
   T = absolute temperature (K)
   R = resistance (Ω)
   W = bandwidth (Hz)
2) Shot noise
   - Is transfer of a quantum of charge and is White and Gaussian noise

   $I_{noise}\,(rms) = \sqrt{2qIDCW}$

   Where, q = $1.60X10^{-19}$ C
   I_{DC} = DC current (A)
   W = measurement bandwidth (Hz)
3) Flicker or Pink noise
   - Flicker, 1/f or "pink" noise varies with frequency

   $V_{noise}\,(rms) = V_f[0.392 + \log_{10}(f_{high}/f_{low})]$

   Where, V_f = noise at a fixed frequency $[V/(Hz)^{1/2}]$
   f_{high} = high frequency corner of bandwidth (Hz)
   f_{low} = low frequency corner of bandwidth (Hz)
4) Interference
   - Coupling of unwanted energy into a device from outside sources.

   $V_{total} = (V_1^2+V_2^2+ \dots +V_n^2)^{1/2}$

   Where, V_{total} = total noise (V)
   $V_1, V_2, \dots, V_n$ = individual noise components (V)

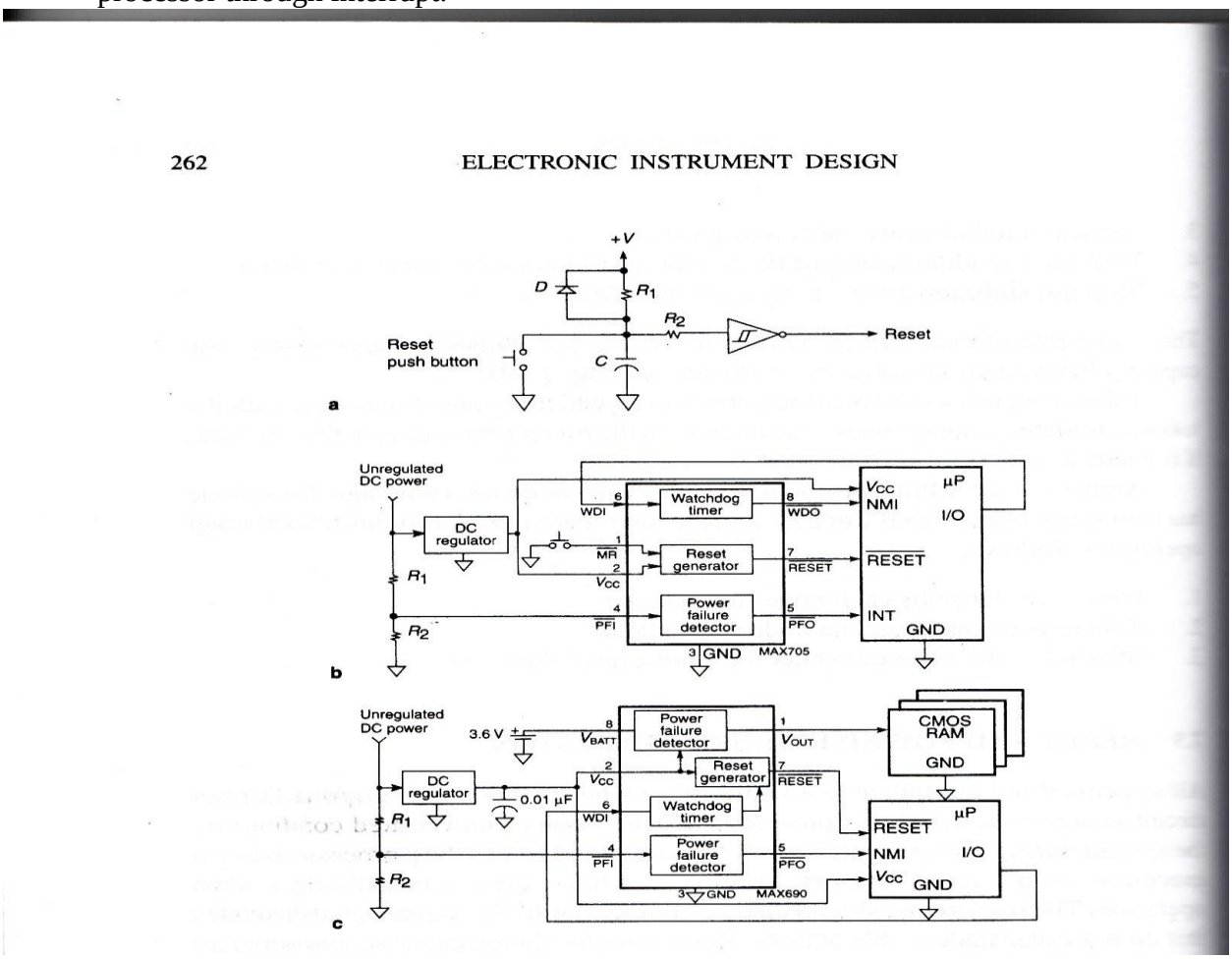
- Quantization error

SNR = $10 \log_{10} (V_{signal}^2/V_{noise}^2)$

Where SNR = signal to noise ratio
V_{signal} = full scale amplitude of the signal (V)
V_{noise} = total noise amplitude of the signal (V)

7.5 Reset and power failure detection and interface unit

- All systems should initialize to a known state whenever power is applied
- Reset circuit generates a signal that prevents the generation of unwanted conditions by the system during power application
- Reset signal
  - Forces the processor to begin execution from a fixed memory location where code for initialing system operation is written.
  - Sets or clears critical output signals to states that don't cause undesirable actions
- Reset circuit senses voltage level and generate reset signal when the voltage of power supply goes below the preset values and the reset signal stays active until the voltage of the power supply exceed the preset value.
- E.g. RC network, watchdog timer
- Some system may turn on the battery backup after power failure and also inform the processor through interrupt.



- The simple reset circuit as in figure uses the time constants R, C network to set the desired duration of the reset signal.
- The Schmitt trigger inverter transforms the exponential changing waveform on the input to a signal transition appropriate for logic gates.
- The diode D allows charge to drain off the capacitor if the DC voltage fails, thereby protecting the inverter from an input voltage higher than its supply voltage.

- When pressed, the manual push button shorts the charge on the capacitor to ground to generate a reset signal so that a user can initialize the operation of the system even while the supply power is stable.

Interface Unit

- The input to all circuit is some sort of electrical signal
- Each signal comes from another circuit, a transducer or a switch.
- Most signals need some preprocessing or conversion before the system can assimilate them
- E.g. Switch generates logic transitions that bounce when pressed; there is a series of rapid glitches at the beginning and end of signal pulse.
- It is necessary to design some circuitry to suppress the glitches produced by bounce.
- Also sensors produce continuously changing analog signal that must be converted to digital logic levels for further processing
- You will need to define the types of inputs that you expect the system will receive
- Once you know the type of input, you can decide on the necessary circuitry to manipulate the input signals.